

# Dynamic input capacitance of single-electron transistors and the effect on charge-sensitive electrometers

Neil M. Zimmerman<sup>a)</sup>

*National Institute of Standards and Technology, Gaithersburg, Maryland 20899*

Mark W. Keller

*National Institute of Standards and Technology, Boulder, Colorado 80303*

(Received 4 January 2000; accepted for publication 17 March 2000)

We examine the “input capacitance,”  $C_{\text{SETT}}$ , of a single-electron tunneling (SET) transistor. We note that this quantity is crucial in quantifying the sensitivity of a SET transistor used as a charge electrometer. Further, we point out that  $C_{\text{SETT}}$  is not the same as the “gate capacitance,”  $C_G$ , usually taken to be  $e/\Delta V_G$ , where  $\Delta V_G$  is the period of the oscillation in current versus gate voltage. While  $C_G$  is indeed the average value of  $C_{\text{SETT}}$  over one period,  $C_{\text{SETT}}$  can in fact differ substantially from that value, depending on the applied voltages. This has important consequences for maximizing the sensitivity of SET charge electrometers when a large stray capacitance is present. [S0021-8979(00)07812-9]

## I. INTRODUCTION AND MOTIVATION

In the past decade, electronic devices based on metal–insulator–metal tunnel junctions, using the Coulomb blockade<sup>1,2</sup> of electrons, have been fabricated with standard thin-film lithography and processing techniques. The Coulomb blockade refers to the fact that, at sufficiently low temperatures and for sufficiently small devices, electrons can tunnel onto or off of an isolated metal island only in units of one. Here, the size and temperature must satisfy the criterion  $kT \ll e^2/2C_\Sigma$  to prevent thermal smearing; the size constraint is driven by the necessity to minimize the total island capacitance,  $C_\Sigma$ , which is typically of order 0.1 fF (corresponding to a Coulomb energy  $e^2/2C_\Sigma$  of order 1 meV or 10 K).

Single-electron tunneling (SET) transistors are three-terminal devices based on two tunnel junctions in series, with a separate capacitive gate to the central island [see Fig. 1(a)]. A basic manifestation of the Coulomb blockade is that, for certain values of voltages  $V_G$  and  $V_{S-D}$ , very little current will occur from source to drain—the flow is “blocked.”

For instance, in the Fig. 1(b), we see that the current  $I_{S-D}$  between source and drain oscillates between minimum (the blocked regime) and maximum, with a period that corresponds to increasing by one the average number of electrons on the island. This “SET oscillation” is the basic device modulation that affords the potential as a charge electrometer: One can typically resolve a relative change in  $I_{S-D}$  of less than or order  $10^{-3}$ , and thus can measure a charge flow onto the gate capacitance of less than or of order  $10^{-3}e$ . This exquisite sensitivity is about five orders of magnitude better than conventional solid-state metal–oxide–semiconductor field-effect transistor (MOSFET)-type transistors.

One of the practical requirements of the SET transistors is that, because the total SET island capacitance<sup>3</sup>  $C_\Sigma = 2C_T + C_G$  must be kept small, the gate capacitance,  $C_G$ , must be small; typically, the maximum value is about 1 fF.<sup>4</sup> This small value can cause a very large decrease in the sensitivity of the SET transistor as a charge electrometer, because most of the charge will flow to the (typically much larger) stray capacitance to ground. As an example, one application (which NIST is presently pursuing) is to develop a capacitance standard based on electron counting;<sup>5,6</sup> in this case, we have the exact situation of a SET electrometer with a large parallel stray capacitance limiting the sensitivity.<sup>4</sup> In fact, the sensitivity is decreased by about a factor of  $10^4$  due to the stray capacitance,<sup>4</sup> and the overall resolution of this standard is presently limited by the electrometer sensitivity.<sup>6</sup>

A generic schematic of this situation will be as shown in Fig. 2(a), with the addition of the elements outside the dotted box. Here, we have denoted a charge source as a voltage source,  $V_C$ , and the coupling capacitor,  $C_C$ , together with the stray capacitance to ground,  $C_{\text{stray}}$ , (a single lumped element representing the charge distributed along the wiring). Typical minimum values for  $C_{\text{stray}}$  are of order 10 fF for both charge source and electrometer microscopic elements on the same chip (substrate), and 10 pF for wiring between charge source and electrometer running off the chip.<sup>7</sup> Note that these minimum values are much larger than the typical maximum  $C_G$  of 1 fF.

The result of the large ratio between  $C_{\text{stray}}$  and  $C_G$  is that, as mentioned above, most of the charge from a change in  $V_C$  or  $C_C$  will flow to  $C_{\text{stray}}$ , not  $C_G$ . We now define the input capacitance,  $C_{\text{SETT}}$ , of the SET electrometer as indicated in Fig. 2(b):  $C_{\text{SETT}}$  is the effective capacitance between the gate capacitor and ground, or in terms of the parameters in Fig. 2(a),  $C_{\text{SETT}} \equiv dQ_G/dV_G$ . It is a dynamic capacitance in the sense that, as we shall shortly see,  $C_{\text{SETT}}$  changes its value as the gate voltage,  $V_G$ , changes (or equivalently from a change in  $V_C$  or  $C_C$ ).

<sup>a)</sup>Electronics and Electrical Engineering Laboratory, Technology Administration, U.S. Department of Commerce; Electronic mail: neil.zimmerman@nist.gov; URL: <http://www.eeel.nist.gov/811/gemg/set.html>

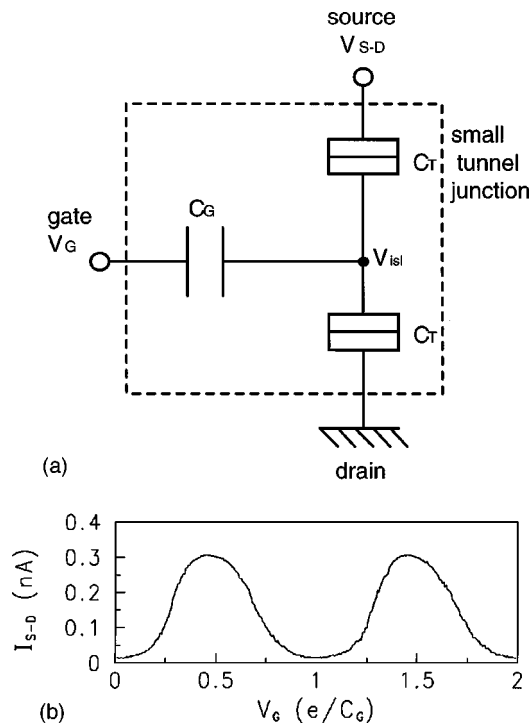


FIG. 1. (a) A schematic of a SET transistor. The two tunnel junctions isolate the central SET island. For the appropriate choices of parameters, the net number of electrons on the island is quantized in units of one, because there is insufficient energy for an extra electron to tunnel onto or off of the island. (b) Example of a measurement of source-drain current,  $I_{S-D}$ , versus gate voltage,  $V_G$ , showing the periodic modulation; each period corresponds to increasing the average number of electrons on the island by one.

We note that, for most applications we have in mind (including the electron counting capacitance standard), the SET electrometer will be used as a null detector with feedback, so that the measurement is of a charge  $Q_C$  or  $Q_G$  which is not changing. For example, in Fig. 2(a), we would feedback a control signal that would result in maintaining  $Q_C$ , the charge on  $C_C$ , at a fixed value; in this sense the electrometer is used as a null detector, only measuring changes in  $Q_G$ . Thus, the application does not in general require an *accurate* measurement of  $Q_C$  (which would require accurate knowledge of  $C_{\text{stray}}$  and  $C_{\text{SETT}}$ ); rather, we only require the ability to resolve a small change in  $Q_C$ , in order to perform the function of a null detector. Thus, the sensitivity we discuss herein refers to a minimum resolution of change in  $Q_C$  or  $Q_G$ .

It is now clear from Fig. 2(b) how the stray capacitance decreases the sensitivity: the charge which we wish to sense,  $Q_C$ , is split into the charges on the stray and gate capacitances as indicated. It easy to show that

$$Q_G = Q_C [C_{\text{SETT}} / (C_{\text{SETT}} + C_{\text{stray}})] \approx (C_{\text{SETT}} / C_{\text{stray}}) Q_C \ll Q_C; \quad (1)$$

note that  $C_{\text{SETT}} / C_{\text{stray}}$  is a small fraction.

## II. INPUT CAPACITANCE: SIMPLE CONSIDERATIONS

We now wish to estimate  $C_{\text{SETT}}$  in terms of the known parameters. There are two obvious possibilities:

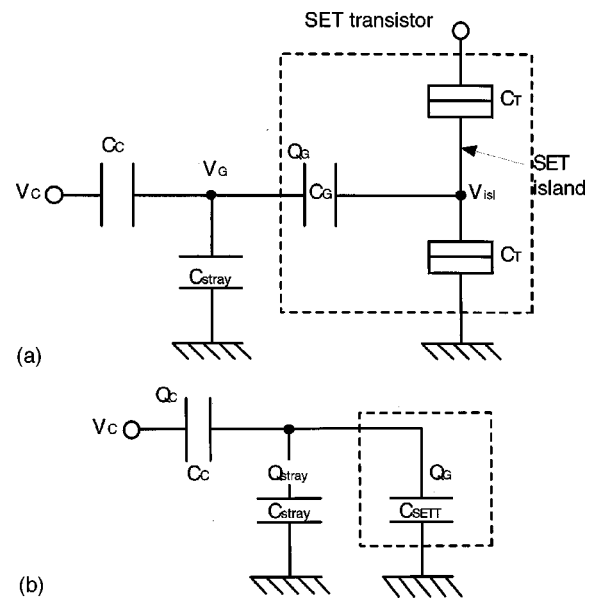


FIG. 2. (a) A schematic of a SET transistor as a charge electrometer. The charge source is represented as a voltage source  $V_C$  followed by a coupling capacitor,  $C_C$ . (b) A schematic of the SET transistor with all of the capacitances lumped into  $C_{\text{SETT}}$ . A change in either  $V_C$  or  $C_C$  causes a charge  $Q_C$  to flow to the common node. This charge distributes itself on the stray and gate capacitances as indicated.

(1) For large amounts of charge transfer such that  $Q_G \gg 1e$ , the net change in the potential on the SET island is small compared to the change in  $V_G$ ; essentially all of the extra charge resides on  $C_G$ , and thus the charge-averaged value (averaged over many periods) is

$$C_{\text{SETT}} \approx C_G.$$

This result is the reason that the period of the SET oscillations is  $e/C_G$ .

(2) What is  $C_{\text{SETT}}$  for small amounts of charge transfer? The answer is that it depends, via the details of the tunneling through the tunnel junctions, on the value of the island potential,  $V_{\text{isl}}$ . In particular, we note that, from Fig. 2(a), it is clear that  $Q_G = C_G(V_G - V_{\text{isl}})$ .

When there is no tunneling (i.e., the blockaded region), the tunnel junctions appear as if they are pure capacitors, and in that region an expression for  $C_{\text{SETT}}$  results simply from the parallel-series combination of capacitances<sup>3</sup> (we can set the source potential to ground without loss of generality):

$$C_{\text{SETT}} \approx \frac{2C_T}{C_G + 2C_T} C_G. \quad (2)$$

We note that this estimate of  $C_{\text{SETT}}$  is always less than  $C_G$ . We also note that, in order to maximize sensitivity while minimizing thermal smearing, the general tendency would be to fabricate a device with relatively large  $C_G$  and small  $C_T$ . This implies that we will often have the situation where  $C_{\text{SETT}} \ll C_G$ .

We can also estimate  $C_{\text{SETT}}$  in the tunneling (nonblockaded) region: First of all, in order to maintain the average value of  $C_{\text{SETT}}$  as  $C_G$ , it is clear that in this region,  $C_{\text{SETT}}$  must be greater than  $C_G$ . We have  $C_{\text{SETT}} \equiv dQ_G/dV_G = C_G(1 - dV_{\text{isl}}/dV_G)$ . We can obtain a rough estimate for

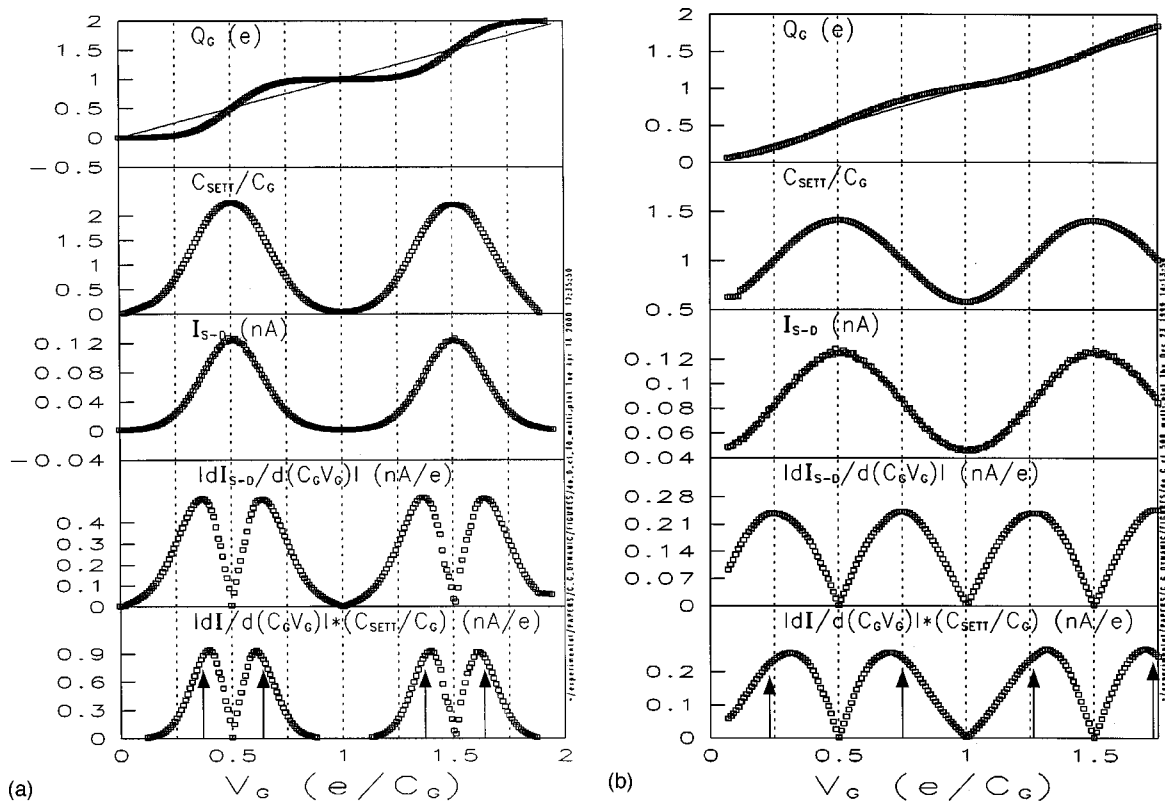


FIG. 3. (a) Top to bottom (see Ref. 8). Gate charge,  $Q_G$ , relative input capacitance,  $C_{SETT}/C_G$ , (derivative of top panel), source-drain current,  $I_{S-D}$ , derivative of  $I_{S-D}$ , and the sensitivity parameter  $\chi = [dI_{S-D}/d(C_G V_G)] (C_{SETT}/C_G)$ , all as a function of  $V_G$ ;  $V_G$  is swept over a range corresponding to a change by two in the average number of electrons on the island [ $\Delta(C_G V_G) = 2e$ ]. The solid line in the top panel is a straight line with a slope of one (corresponding to  $C_{SETT} = C_G$ ). The solid line in the middle panel is a sliding average of the data, from which the derivative in the next panel is calculated. The arrows in the bottom panel denote the positions where the derivative of  $I_{S-D}$  is a maximum. The parameters of this simulation are:  $C_G = 1$  fF,  $C_T = 10$  aF,  $R = 100$  k $\Omega$ ,  $V_{S-D} = 0.05$  mV,  $T = 0.1$  K. The salient features include: (1) the gate charge,  $Q_G$ , is essentially unchanging in the blocked regions (when  $I_{S-D}$  is small), since the input capacitance,  $C_{SETT}$ , is dominated by the tunnel junction capacitances,  $C_T$ , which are much smaller than  $C_G$ ; (2)  $C_{SETT}$  varies from about  $2C_G$  to a small fraction of  $C_G$  [note that  $2C_T/(C_G + 2C_T) \approx 0.02$ ]; (3) the places where the slope of  $I_{S-D}$  is maximized (arrows at bottom) are not where  $\chi$  is maximized. (b) Similar to (a), with tunnel junction capacitance values of 500 aF (Ref. 8).

$dV_{isl}/dV_G$  as follows: with the total island capacitance,  $C_\Sigma \equiv 2C_T + C_G$ , the island potential decreases by about  $(e/2) \times (1/C_\Sigma)$  between minimum and maximum tunneling, and this change occurs over a change in  $V_G$  of about  $1/4(e/C_G)$ . Then, approximating  $V_{isl}(V_G)$  as linear in this region, we get  $dV_{isl}/dV_G \approx (-e/2C_\Sigma)/(e/4C_G) = -2C_G/C_\Sigma$ , or  $C_{SETT} \approx C_G(1 + 2C_G/C_\Sigma)$ ; for a typical value of  $C_T \approx 1/2C_G$ , this will result in  $C_{SETT} \approx 2C_G$ .

### III. INPUT CAPACITANCE: SIMULATIONS

By considering some simple simulations,<sup>8</sup> we can see in some detail how the input capacitance,  $C_{SETT}$ , depends on various parameters. First, we note that the desired measurement is of  $Q_C$ , and thus the salient sensitivity parameter (in the presence of a large  $C_{stray}$ ) is dependent on  $V_G$  and  $V_{S-D}$  by two factors: the first is the uncertainty in the measurement of  $Q_G$ , which is inversely proportional to the slope of the current,  $|dI_{S-D}/d(C_G V_G)|$ . The second is the decrease in the sensitivity due to the stray capacitance [Eq. (1)], proportional to  $C_{SETT}/C_{stray}$ . Thus, we define the sensitivity parameter

$$\chi = |dI_{S-D}/d(C_G V_G)| (C_{SETT}/C_G);$$

we wish to examine the dependence of  $\chi$  on  $V_G$  and  $V_{S-D}$ .

We first look at a fairly extreme example, where  $C_G = 1$  fF, and  $C_T = 10$  aF, seen in Fig. 3(a). We note that, because the temperature of 0.1 K is fairly small compared to the Coulomb energy, the blockade regions are fairly broad and deep (middle panel). Also, because the ratio  $2C_T/(C_G + 2C_T) \approx 0.02$  is fairly small,  $Q_G$  (top panel) appears flat in the blocked regions, and thus the input capacitance (second panel) also has broad regions where it is very small in comparison to  $C_G$ —if we operated the electrometer in these regions, the sensitivity would be decreased by this very small  $C_{SETT}$ .

We note that the positions in  $V_G$  where the slope  $|dI_{S-D}/d(C_G V_G)|$  is maximum (arrows at bottom) are not coincident with the maxima of  $C_{SETT}$ ; thus, the positions to maximize  $|dI_{S-D}/d(C_G V_G)| C_{SETT}$  are not the positions of maximum slope. In fact, in this example, we would lose a factor of about 1/5 in sensitivity if we operated at the positions of maximum slope.

Figure 3(b) shows similar qualitative features, for the

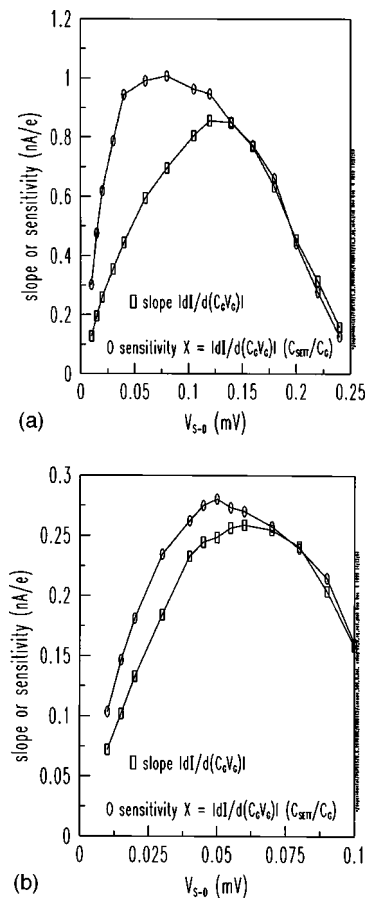


FIG. 4. (a) Dependences (see Ref. 8) of two possible sensitivity parameters (slope of current oscillations and parameter  $\chi$ ), maximized with respect to gate voltage,  $V_G$ , (separately for each data point), as a function of bias voltage  $V_{S-D}$ . Note the (1)  $\chi$  peaks somewhat before the slope and also before the amplitude of current oscillations (not shown), and that (2)  $\chi$  is always bigger than the slope, showing the enhancement due to  $C_{SETT}$ .  $C_G = 1$  fF,  $C_T = 10$  aF,  $R = 100$  k $\Omega$ ,  $T = 0.1$  K. (b) Similar,  $C_T = 500$  aF (see Ref. 8).

case with  $C_T = 0.5$  fF (approximately the values used in the electron-counting capacitor standard experiment).

Finally, Fig. 4 shows dependences of some of these parameters on the bias voltage,  $V_{S-D}$ . To get this plot, for each value of  $V_{S-D}$ , we have used plots like Fig. 3 to find the value of  $V_G$  which maximizes  $|dI_{S-D}/d(C_G V_G)|$  and  $\chi$ ; note that this maximization means that different data points correspond to different values of  $V_G$ . We note that another possible sensitivity parameter, the maximum amplitude of the current oscillation  $\Delta I_{S-D}$ , has a shape very similar to the slope, and thus using the amplitude as the criterion for device operation would lead to the same choice of  $V_{S-D}$  as the slope. We see that, for Fig. 4(a), with  $C_T = 10$  aF, similar to the dependence on  $V_G$  [see Fig. 3(a)], the maxima in these parameters do not occur at the same points. In particular, the amplitude (not shown) and slope reach their maxima at a bias voltage,  $V_{S-D}$ , where  $\chi$  has already lost a fraction of its value. Figure 4(b) shows similar results for the case of  $C_T = 0.5$  fF.

We also note that as expected from the above, the enhancement of  $C_{SETT}$  in the nonblocked regions of  $V_G$

causes the maximum sensitivity to be always be bigger than the maximum slope (although in some regions by no more than 15%).

#### IV. SUMMARY

We have shown that:

(1) Due to the periodic modulation of the island potential,  $V_{isl}$ , the effective input capacitance,  $C_{SETT}$ , varies markedly over one period in  $V_G$ , from a small fraction of the nominal gate capacitance,  $C_G$ , to about twice  $C_G$ .

(2) This periodic modulation of  $C_{SETT}$  has a linearly proportional effect on the sensitivity of a SET transistor used as a charge electrometer, when the stray capacitance to ground is large compared to  $C_{SETT}$  (often the case).<sup>9-11</sup>

(3) Fortunately, the value of  $C_{SETT}$  reaches a maximum in gate voltage quite near the maximum in the derivative of current versus  $V_G$ . Thus, the modulation of  $C_{SETT}$  causes a small enhancement of the overall sensitivity.

(4) As seen in Figs. 3(a) and 4, the choice of the control voltages is more important than might be thought in the absence of this effect, since  $C_{SETT}$  falls off quite rapidly with  $V_G$  and  $V_{S-D}$  in some cases.

As a conclusion, although the enhancement effects in this article appear to be fairly small, they may be significant in cases where the resolution of the experiment is limited by the sensitivity of the electrometer.<sup>6</sup> Perhaps more importantly, by recognizing the effect of  $C_{SETT}$ , we can avoid the mistake of choosing values of the gate or source-drain voltages which at first sight would appear to be close to optimum, but which would significantly degrade the sensitivity.

#### ACKNOWLEDGMENTS

The authors are happy to acknowledge a careful reading of the manuscript by Mike Kelley (NIST Gaithersburg) as well as discussions with Bill Huber, Nick Paulter (NIST Gaithersburg), and Chris Lobb (U. Maryland).

<sup>1</sup>D. V. Averin and K. K. Likharev, *Single Electronics: A Correlated Transfer of Single Electrons and Copper Pairs in Systems of Small Tunnel Junctions* (North-Holland, New York, 1991), Vol. 30, Chap. 6, pp. 173–272.

<sup>2</sup>H. Grabert and M. H. Devoret, *Single Charge Tunneling* (Plenum, New York, 1992), Vol. 294.

<sup>3</sup>Here we have neglected the contribution to the SET island capacitance due to field lines terminating at infinity (i.e., not due to  $C_T$  or  $C_G$ ); this contribution is often quite small, and in any case will simply add to  $2C_T$ , and thus not change any of the general conclusions.

<sup>4</sup>N. M. Zimmerman, J. L. Cobb, and A. F. Clark, *IEEE Trans. Instrum. Meas.* **46**, 294 (1997).

<sup>5</sup>E. R. Williams, R. N. Ghosh, and J. M. Martinis, *J. Res. Natl. Inst. Stand. Technol.* **97**, 299 (1992).

<sup>6</sup>M. W. Keller, A. L. Eichenberger, J. M. Martinis, and N. M. Zimmerman, *Science* **285**, 1706 (1999).

<sup>7</sup>M. W. Keller, J. M. Martinis, N. M. Zimmerman, and A. H. Steinbach, *Appl. Phys. Lett.* **69**, 1804 (1996).

<sup>8</sup>Simulation results obtained using the software package SIMON (<http://homel.gte.net/kittypaw/index.htm>) developed by Christoph Wasshuber. The identification of a specific commercial product does not imply endorsement by NIST, nor does it imply that the product identified is the best available for a particular purpose.

<sup>9</sup>The sensitivity of a transistor must be considered in the context of the noise floor. For SET transistors, the dominant intrinsic noise is  $1/f$  charge

noise. If this charge noise arises from sources in the tunneling junctions or near the island (typically the case), the noise level will be unaffected by  $C_{\text{SETT}}$  and thus the sensitivity will indeed be linearly proportional to  $C_{\text{SETT}}$ . In contrast, if the noise arises from sources which couple through  $C_G$ , then the noise level will be affected by  $C_{\text{SETT}}$  in the same way as the signal, and thus the ratio of signal to noise will not depend on  $C_{\text{SETT}}$ . For

more on the location of charge noise sources in SET transistors. See Refs. 10 and 11.

<sup>10</sup>N. M. Zimmerman, J. L. Cobb, and A. F. Clark, Phys. Rev. B **56**, 7675 (1997).

<sup>11</sup>A. B. Zorin, F.-J. Ahlers, J. Niemeyer, T. Weimann, H. Wolf, V. A. Krupenin, and S. V. Lotkhov, Phys. Rev. B **53**, 13 682 (1996).